ABSTRACT OF THE DISCLOSURE

A protection layer is formed on a transparent substrate having a plurality of thin film transistors, and an exposure step is then carried out by means of a half-tone mask. An outer lead bonding area is located on the periphery of the transparent substrate. After the exposure and development steps, most of the protection layer in the outer lead bonding area is removed. With an etching step, the top of an insulation layer of the outer lead bonding area is exposed and a plurality of via holes are formed in the insulation layer, thus a metal layer is exposed from the via holes as outer lead bonding pads. Finally, a transparent conductive layer with desired patterns is formed on the protection layer, and the transparent conductive layer is extended into the via holes of the protection layer to connect with the thin film transistors.